ELLIOTT 900

Volume 4: ENGINEERING MAINTENANCE

Part 3: OPTIONAL UNITS

Section 3: 4100 INTERFACE MATCHING UNIT

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END-OF-TEXT FIGURES

Fig.

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Chapter 1: GENERAL

1.1 Introduction

The 900/4100 Interface Matching Unit is designed so that peripheral devices having a 4100 interface can be used with the 900 system. The IMU can be connected to the central processor via the general peripheral socket or via a multiplexer.

The IMU is a self contained unit which can be housed on three shelves of a standard 900 desk. The layout of the unit is shown in Figure 1.

The IMU can be provided with facilities for 2, 4, 6 or 8 devices to be used. The logic rack is fully wired for the maximum of 8 devices, so that a small system can be expanded by the addition of the required logic boards. The logic boards required for the various sizes are listed on Figure 1.

Additional information can be obtained from Section 1.2.7. 900 Standard Peripheral Interface and 1.3.3. 4100 Interface Matching Unit.

1.2 Connections

Each interface channel has one cable connecting the device to the IMU.

The IMU is connected to the central processor via two cables. One cable carries input and output data and control signals, the second cable carries control signals only.

The plugs and sockets associated with the IMU are mounted on an entry panel as shown in Figure 1.

1.3 Logic Drawings

The circuits of the L. S. A. elements used on the logic boards are shown and described in Section 4.1.1. The tables in Figure 10 provide details of the types of L. S. A. element on each board and the location and value of any extra components used.

On the logic diagrams, signals to and from the central processor are enclosed in square brackets [ ] and signals to and from the peripheral devices are enclosed in diamond brackets < >. All discrete components, not being part of the logic sub-assemblies, are fitted in Area G of the logic board.

In the text, references to the positions of logic elements will generally take the following form.

EXAMPLE: "8/7A11" refers to a logic sub-assembly on the logic board in slot position 8. It will be part of the L. S. A. in area 7A on that board and will be the logic element whose output pin is numbered 11.

Chapter 2: POWER SUPPLIES

2.1 Introduction

The power supply equipment occupies one rack of the IMU assembly. The d.c. supplies are provided by two separate proprietary units. Details of these can be obtained from the manufacturers handbooks. A mains filter unit and a d.c. over-voltage protection circuit are also incorporated. The relative positions of the units in the rack can be seen in Figure 1.

2.2 D.C. Supplies

The d.c. supplies required by the logic boards are +6 Volts and -6 Volts. The +6 Volts is provided by PU1, Catalogue No. 11258, the output line being fused at 3A. The -6 Volts is provided by PU2, Catalogue No. 11186, the output line being fused at 1A. Figure 2 shows the connections within the power chassis and the distribution of the d.c. supplies to the logic rack.

2.3 Over-Voltage Protection

An over-voltage protection circuit is connected across the +6 Volts and -6 Volts d.c. outputs to protect the logic boards from damage due to a rise in level of either of these supplies. Under normal operating conditions, no current is taken by the circuit.

If either of the d.c. outputs start to rise then current will be drawn through the corresponding zener diode and current applied to the thyristor. Dependent on the ambient temperature and component tolerances, the thyristor will be triggered when the d.c. level has risen to a value between 6.5 Volts and 10.0 Volts.

When the thyristor conducts, the output terminals of the power unit are short circuited causing the appropriate fuse to blow.

Chapter 3: LOGIC DESCRIPTION

3.1 Introduction

This chapter contains a functional description of the logic associated with the 900/4100 Interface Matching Unit, when used to transfer data in either direction between a peripheral device and the central processor. The unit can provide facilities for up to eight peripheral devices to be used. The logic rack is wired to accommodate the maximum number of channels, so that a small unit can be expanded by the addition of the required logic boards. The diagrams in this Section show the complete logic for an eight channel IMU.

3.2 Modes of Operation

The IMU can transfer data in either direction in one of three ways, the mode of operation being determined by the address lines from the central processor.

(a) Single unpacked in which an 8-bit character is transferred.

(b) Unpacked repetitive in which a series of 8-bit characters are transferred.

(c) Packed repetitive in which a series of 18-bit characters are transferred.

3.3 Typical Input Cycle

A simplified description of the sequence of events when a single character is input to the central processor is as follows:-

An input select signal sets the control logic to the required state, resets the buffer register and produces a pulse to commence the data transfer.

The starting pulse causes a request to be sent to the peripheral, which then places the data onto the interface lines and sends a response back to the IMU. This causes the IMU to gate the data from the lines into the buffer register and therefore the data appears on the processor interface lines.

A reply is sent to the processor which then strobes the data from its interface lines and removes the input select signal.

3.4 Typical Output Cycle

In a simplified description of a single output transfer the processor places the data onto its interface lines and sends an output select signal to the IMU. The control logic is set by this signal, and the buffer register reset and then loaded with the output data.

The transfer to the peripheral is then started by gating the data onto the peripheral interface lines and sending a request to the device. When the data has been accepted by the device it sends a response back to the IMU, and a reply is sent to the processor. The processor then removes the output select signal.

3.5 Channel Selection

The channel of the IMU that is to be used is determined by the state of the signals [OS1], [OS2] and [OS3] from the central processor. The logic is shown in Figure 8.

The interface signals are fed to the receiving elements 2/5B11, 2/5B12 and 2/5B13 where they are inverted to produce $\overline{D1}$, $\overline{D2}$ and

$\overline{D3}$. A further inversion at 2/3A11, 2/3A12 and 2/3A13 produces D1, D2 and D3.

The D and $\overline{D}$ signals are fed in combinations of three to the channel selection gates 2B12 and 1B12 on boards 12, 14, 17 and 19. They are gated with SEND, which goes true for both input and output modes of operation. When a selection gate is opened, true <MASK> and M signals are produced from 5A13 and 2B13 or 5A11 and 2B11 on the respective board. The <MASK> signal is fed to the peripheral device, the M signal is used within the IMU.

The combinations of the D signals are such that the interface signals must be in the state specified for that channel to be selected.

Channel 1 - all false	5 - [OS3] true
2 - [OS1] true	6 - [OS1] and [OS3] true
3 - [OS2] true	7 - [OS2] and [OS3] true
4 - [OS1] and [OS2] true	8 - all true.

3.6 Buffer Register

The buffer register consists of three type DP43 boards located in positions 8, 9 and 10 of the logic rack. Each board contains six bistables giving a register capable of holding 18 data bits. The logic is shown in Figure 5. The data receivers and transmitters feeding the information between the peripheral devices and the register are shown in Figure 7.

Taking bit 1 as a typical example, the output from the central processor [OA1] is inverted by the receiver 8/7A11 and also by 8/5A11. The resultant signal is gated with LOAD/2 to set the bistable 8/4A13, 8/1A11 causing DATA1 to go true. OUTC is gated with DATA1 at

11/1A13 to place the information onto the peripheral line via the transmitter element 13/4A13.

On an input transfer the peripheral device places the information on the <DATA IN> lines. Again using bit 1 as the example, the signal is inverted by the receiver 13/1A13 and by 11/1B11 to produce DIN1. This signal is gated with INC to set the bistable 8/4A13, 8/1A11 and place the data onto the processor interface line [IG1] via the transmitter element 8/6A11.

The status word data bits $\overline{X1}$ to $\overline{X18}$ are fed directly to the transmitter elements 8/6A11 etc. and hence onto the interface lines.

3.7 Control Counter

3.7.1 General

The logic for the counter is located on boards type DP40 and DP41 in positions 5 and 6 respectively of the logic rack and is shown in Figure 4. The outputs Z1, $\overline{Z1}$, Z2 and $\overline{Z2}$ are gated on board 6/DP41 to produce A, B, C and FULL which control the sequence of the data transfer. When the IMU is first switched on the state of the counter is undefined and is set at the start of the first data transfer.

3.7.2 Unpacked Transfer

In the unpacked mode of operation it is required that C be made true for the duration of the transfer and that FULL then be made true. This occurs for both input and output in the single and repetitive modes.

At the start of a data transfer a true CLEAR* pulse is generated by 4/2A13 (Figure 3). This pulse is inverted by 5/7A11 to set the bistable 5/5B12, 5/5B13 so that $\overline{Z1}$ is true.

In the unpacked mode of operation, UNPACKED is true so that CLEAR* going true causes the output of 5/7A13 to go false to set the bistable 5/5A12, 5/5A13 so that Z2 is true. UNPACKED and CLEAR* gated at 5/5A11 set the bistable 5/3B11, 5/2B11 such that the output of 5/2B11 is true.

Z2 and $\overline{Z1}$ fed to 6/4A12 cause C to go true. A, B and FULL are false.

When a <RESPONSE> is received from the peripheral device, $\overline{RESPA}$ or $\overline{RESPB}$ goes false causing $\overline{RESP}$ to go false and 5/2A11 to produce a 0.4 μsec. PREP* pulse. This pulse is gated with $\overline{Z1}$ at 5/2B13 causing its output to go false to set the bistable 5/2B12, 5/3B13 to that the output of 5/2B12 is true. The pulse does not affect the gates 5/6B13, 5/6A13 and 5/6A11.

When the pulse ends, a delay of 0.4 μsec, produced by 5/2A13, occurs before a 0.4 μsec. COUNT pulse is generated by 5/4A11.

The COUNT pulse gated with the true output of 5/2B12 at 5/7B13 resets the bistable 5/5B12, 5/5B13 so that Z1 is true.

The C signal goes false and Z1 and Z2 fed to 6/4A11 cause FULL to go true.

At the end of COUNT, 5/4A13 is triggered to produce the 0.4 μsec DONE pulse.

3.7.3 Packed Transfer

The packed transfer of data requires that the counter produces signals in the order A, B, C and FULL for input and output modes of operation. The PACKED signal is made true and after a select signal is received the CLEAR* pulse is generated from 4/2A13 (Figure 3).

As in the unpacked transfer the CLEAR* pulse fed to 5/7A11 sets the bistable such that $\overline{Z1}$ is true. PACKED, $\overline{SW}$ and CLEAR* cause the output of 5/1B12 to go false and reset the bistable 5/5A12, 5/5A13 so that $\overline{Z2}$ is true. The bistables 5/3B11, 5/2B11 and 5/2B12, 5/3B13 are also set such that the outputs of 5/3B11 and 5/3B13 are true.

$\overline{Z1}$ and $\overline{Z2}$ are fed to 6/5B13 cause A to go true.

On receipt of a true <RESPONSE> signal from the peripheral $\overline{RESP}$ goes false and a 0.4 μsec PREP* pulse is produced by 5/2A11. This pulse is gated with $\overline{Z1}$ at 5/2B13 to set true the bistable output 5/2B12.

When the pulse ends, a delay of 0.4 μsec is introduced by 5/2A13 before the 0.4 μsec COUNT pulse is generated by 5/4A11. The true output of 5/2B12 is gated with COUNT at 5/7B13 to set Z1 true.

The A signal goes false and Z1 and $\overline{Z2}$ cause B to go true via 6/4A13.

The next <RESPONSE> signal causes 5/2A11 to generate PREP*. PREP* gated with Z1 at 5/6B13 sets the output of bistable element 5/3B13 to a true level. The pulse is also gated with Z1 and $\overline{Z2}$ at 5/6A13 to set true the output of bistable element 5/2B11.

When the COUNT pulse occurs it is gated with the true bistable outputs at 5/5B11 and 5/7B12 to set the Z2 bistable and reset the $\overline{Z1}$ bistable.

The B signal goes false and $\overline{Z1}$ and Z2 fed to 6/4A12 cause C to go true.

The third <RESPONSE> signal again produces PREP*. PREP* gated with $\overline{Z1}$ at 5/2B13 causes the output of bistable element 5/2B12

to go true. The COUNT pulse is gated with the true output of 5/2B12 at 5/7B13 causing the Z1 bistable to be set and Z1 to go true.

The C signal goes false and FULL is made true by Z1 and Z2 via 6/4A11.

At the end of COUNT, 5/4A13 is triggered to produce the 0.4 μsec DONE pulse.

3.8 Single Unpacked Output

3.8.1 Initial Setting (Figure 3)

On a single unpacked output transfer, the central processor makes the address signals [OS10], [OS11] and [LW] true. The channel required is selected by making [OS1], [OS2] and [OS3] true as detailed in para. 3.5. The data is placed on the interface lines [OA1] to [OA8] and [SOP] is made true. A typical waveform diagram is shown in Figure 6.

[SOP] is inverted by 2/6B13 and 2/4B13 to give a true OPREQ signal.

PACKED and IPREQ are false causing the output of 2/2B12 to be true and therefore $\overline{SW}$ to be true. [OS10] and [OS11] are true and [OS8] and [OS9] false causing the output of 2/2A12 to be false. This false output is inverted by 2/2A11 and gated with $\overline{SW}$ and OPREQ at 2/1B13 causing the output to go false and REQ and OPQ to go true.

With [LW] true, when REQ goes true the output of 1/3B13 goes false to trigger 1/4A13 and produce a 1.2 μsec pulse. The end of this pulse triggers 1/4B13 to generate a 0.5 μsec pulse to set the bistable 1/6A13, 1/5A12 so that $\overline{END}$ is false. The bistable 1/2B13, 1/2B11 is also set so that END* is true.

After two inversions REQ is gated with $\overline{\text{INH I/O}}$, the true output of the bistable element 3/7A12, to trigger 3/3B13 and produce the 1.4 μsec SET I/O pulse. The pulse is fed to 4/4B13 causing its output to go false and hence $\overline{\text{CLEAR/1}}$ and $\overline{\text{CLEAR/2}}$ go false. These two pulses reset the buffer register bistables on boards 8, 9 and 10 (Figure 5).

After two inversions the SET I/O pulse is gated with OPQ at 3/2B11 giving a false output to set the bistable 3/2B12, 3/2B13 so that OUTPUT is true. This signal is inverted by 3/7A13 causing INPUT to go false. INPUT is fed to boards 12, 14, 17 and 19 (Figure 8) causing a true <OUTPUT> signal to be sent to each peripheral device.

A further inversion of SET I/O at 3/4B11 triggers 3/2A13 causing $\overline{\text{RSW}}$ to go false for 0.4 μsec. The output of 3/2A13 is inverted by 3/4B12 to trigger 3/4A13 and produce the 0.4 μsec RSRY pulse. $\overline{\text{RSW}}$ is fed to board 7 (Figure 9) ensuring that the bistable 7/5B12, 7/5B13 is set so that TOK and $\overline{\text{X18}}$ are true and bistable 7/5A12, 7/5A13 is set so that $\overline{\text{X17}}$ is true. RSRY inverted by 6/4B11 ensures that bistable 6/4B12, 6/4B13 is set so that [PR] is false.

At the end of the SET I/O pulse, 3/2A11 is triggered to generate a 0.4 μsec pulse to set the bistable 3/1B12, 3/1B13 causing $\overline{\text{SEND}}$ to go false. This signal sets the bistable 3/7A12, 3/7A11 so that $\overline{\text{INH I/O}}$ is false and inputs to the pulse generator 3/3B13 are inhibited.

3.8.2 Data to Register

SEND, the output of 3/5B13 is gated with REQ and FREE at 4/6A13 to produce a false output to trigger 4/2A13 and generate a 0.5 μsec CLEAR* pulse. The CLEAR* pulse is fed to board 5 (Figure 4) to set the control counter, as described in para. 3.7.2, so that C is true and FULL is false.

CLEAR* is inverted twice and gated with OPQ at 4/3A12 causing LOAD/1 and LOAD/2 to go true for 0.5 μsec. These two pulses are fed to boards 8, 9 and 10 (Figure 5) and gated with data signals DIN1 to DIN8 to load the buffer register bistables, (see para. 3.6).

The end of the CLEAR* pulse triggers 4/1B11 to produce a delay pulse of 0.4 μsec width, before 4/1B13 generates a 0.4 μsec RS pulse.

3.8.3 Data to Peripheral

RS and $\overline{SW}$ gated at 4/1A12 cause $\overline{START}$ to go false to reset the bistable 4/5B11, 4/5B13 so that FREE goes false. $\overline{START}$ also sets the bistable 4/7B11, 4/7B12 so that TRANSFER goes true.

OUTPUT and TRANSFER gated at 3/1A12 cause OUT to go true. This signal is fed to 11/3B13 (Figure 5) and gated with C to cause OUTC to go true. The outputs of the buffer register bistables, DATA1 to DATA8, are gated with OUTC to place the information onto the peripheral interface lines <DATA OUT1> to <DATA OUT8>, via the transmitter elements on boards 13, 15, 18 and 20 (Figure 7).

TRANSFER gated with C and END* at 7/4B13 causes $\overline{41END}$ to go false. A true <END> signal is therefore sent to each peripheral via the transmitter elements on boards 12, 14, 17 and 19 (Figure 8).

TRANSFER is also gated with C, REQ and $\overline{RESP}$ at 7/3A12 causing the output to go false and trigger 7/2B13. This produces a delay pulse of 0.7 μsec before 7/3B13 is triggered to generate a 0.7 μsec pulse to set the bistable 7/7A12, 7/7A13 causing $\overline{41REQ}$ to go false. A true <REQUEST> signal is sent to each peripheral via the transmitter elements on boards 12, 14, 17 and 19 (Figure 8).

The peripheral selected by the address lines [OS1] to [OS3] will now accept the data from the lines and send a true <RESPONSE> signal to the IMU.

3.8.4 Operation of Counter

The <RESPONSE> signals are received on boards 12, 14, 17 and 19 (Figure 8) where they are inverted twice and then gated with the M signal derived from the channel selection logic. $\overline{\text{RESPA}}$ or $\overline{\text{RESPB}}$ goes false and these signals fed to 5/1A12 cause $\overline{\text{RESP}}$ to go false and 5/2A11 to be triggered (Figure 4). The 0.4 μsec pulse primes the control counter (see para. 3.7.2), and causes PREP to go true and $\overline{\text{PREP}}$ false.

$\overline{\text{PREP}}$ resets the Transfer bistable. The true <END> signal is therefore removed from the peripheral lines and OUTC going false removes the data signals.

PREP gated with C and OPQ at 4/5A11 causes $\overline{\text{CLEAR/1}}$ and $\overline{\text{CLEAR/2}}$ to go false to reset the buffer register bistables on boards 8, 9, and 10.

At the end of the PREP* pulse, 5/2A13 is triggered to generate a 0.4 μsec delay pulse before 5/4A11 produces the 0.4 μsec COUNT pulse. This pulse steps the control counter so that C goes false and FULL true.

3.8.5 End of Transfer

At the end of the COUNT pulse, 5/4A13 produces the 0.4 μsec DONE pulse. This pulse gated with END* and FULL at 3/5A11 resets the Send bistable. DONE, FULL and OUTPUT gated at 4/5A13 sets the Free bistable. DONE is inverted at 7/2A11 and the false pulse used to reset the bistable 7/7A12, 7/7A13 to cause the <REQUEST> signal to go false.

DONE, END*, FULL and OPQ gated at 6/2A12 cause $\overline{\text{SETRY}}$ to go false to set the bistable 6/4B12, 6/4B13 and send a true [PR] signal to the central processor.

When the central processor makes [SOP] false, REQ goes false to trigger 3/4A11. This in turn triggers 3/4A13 to produce the 0.4 μsec RSRY pulse. The pulse is inverted by 6/4B11 and used to reset the bistable 6/4B12, 6/4B13 causing [PR] to go false.

REQ going false also resets the bistable 3/7A11, 3/7A12 causing $\overline{\text{INH I/O}}$ to go true and remove the inhibit from pulse generator 3/3B13.

The logic is now ready to accept the next data transfer.

3.9 Repetitive Packed Output

3.9.1 Setting Control Logic

In this output mode the central processor makes address lines [OS7], [OS10], [OS11] and [BT] true. The channel required is selected by [OS1], [OS2] and [OS3] as described in para.3.5. The data is placed on the interface lines [OA1] to [OA18] and [SOP] is made true. A typical waveform diagram is shown in Figure 6.

[SOP] is inverted by receiver 2/6B13 and by 2/4B13 to give a true OPREQ signal.

IPREQ is false causing the output of 2/2B12 to be true and therefore $\overline{\text{SW}}$ to be true. [OS10] and [OS11] are true and [OS9] and [OS8] are false causing the output of 2/2A12 to be false. This false output is inverted and gated with $\overline{\text{SW}}$ and OPREQ at 2/1B13 causing the output to go false and hence REQ and OPQ go true.

After two inversions REQ is gated with $\overline{\text{INH I/O}}$, the true output of bistable element 3/7A12, to trigger 3/3B13 and produce the 1.4 μsec SET I/O pulse. The pulse is fed to 4/4B13 causing the output to go false and hence $\overline{\text{CLEAR/1}}$ and $\overline{\text{CLEAR/2}}$ to go false. These two pulses reset the buffer register bistables on boards 8, 9 and 10 (Figure 5).

SET I/O gated with BLOCK at 1/5B11 produces a negative pulse to reset the End and End* bistables.

After two inversions the SET I/O pulse is gated with OPQ at 3/2B11 producing a false output to set the bistable 3/2B12, 3/2B13 so that OUTPUT is true. This signal is inverted by 3/7A13 causing INPUT to go false. INPUT is fed to boards 12, 14, 17 and 19 (Figure 8) causing a true <OUTPUT> signal to be sent to each peripheral device.

A third inversion of SET I/O by 3/4B11 causes 3/2A13 to trigger and produce the 0.4 μsec $\overline{\text{RSW}}$ pulse. The pulse is inverted by 3/4B12 to trigger 3/4A13 causing RSRY to go true for 0.4 μsec. $\overline{\text{RSW}}$ is fed to board 7 (Figure 9) to ensure that the bistable 7/5B12, 7/5B13 is reset so that TOK and $\overline{\text{X18}}$ are true and bistable 7/5A12, 7/5A13 is reset so that $\overline{\text{X17}}$ is true. RSRY inverted by 6/4B11 ensures that bistable 6/4B12, 6/4B13 is reset so that [PR] is false.

At the end of the SET I/O pulse, 3/2A11 is triggered to produce a 0.4 μsec pulse to set the bistable 3/1B12, 3/1B13 causing $\overline{\text{SEND}}$ to go false. This signal sets the bistable 3/7A12, 3/7A11 so that $\overline{\text{INH I/O}}$ is false and inputs to the pulse generator 3/3B13 are inhibited.

3.9.2 Loading Register

SEND, REQ and FREE are gated at 4/6A13 producing a false signal to trigger 4/2A13 and generate the 0.5 μsec CLEAR* pulse. As [OS7] is true, PACKED is true and UNPACKED false. These two signals

with CLEAR* set the control counter, as described in para.3.7.3. so that $\overline{Z1}$ and $\overline{Z2}$ are true and hence A and $\overline{FULL}$ are true.

CLEAR* is inverted twice and then gated with OPQ at 4/3A12 causing LOAD/1 and LOAD/2 to go true. The data on the interface lines [OA1] to [OA18] is fed to boards 8, 9 and 10 (Figure 5) and is gated by the LOAD/1 and LOAD/2 pulses into the buffer register.

When CLEAR* goes false, 4/1B11 is triggered to introduce a 0.4 μsec delay before 4/1B13 produces the 0.4 μsec RS pulse.

RS is inverted by 4/1A11 and 6/1A13 and then gated with OPQ and $\overline{END}$ at 6/1B13 causing $\overline{SETRY}$ to go false. The bistable 6/4B12, 6/4B13 is set and a true [PR] signal sent to the central processor.

3.9.3 First Transfer

RS and $\overline{SW}$ gated at 4/1A12 cause $\overline{START}$ to go false for 0.4 μsec.

$\overline{START}$ resets the Free bistable and sets the Transfer bistable.

TRANSFER is fed to 3/1A12 and gated with OUTPUT causing OUT to go true. A is gated with OUT at 11/7B12 (Figure 5) causing OUTA to go true. The outputs of the buffer register, DATA 13 to DATA 18, are gated with OUTA, at 11/1A13 etc. causing the information to be transferred to the $\overline{DOUT1}$ to $\overline{DOUT6}$ lines. This information is fed to the peripheral interface lines via the transmitter elements on boards 13, 15, 18 and 20 (Figure 7).

TRANSFER, $\overline{C}$ and $\overline{RESP}$ gated at 7/4B11 cause 7/2B13 to be triggered and produce a 0.7 μsec delay pulse before 7/3B13 is triggered.

The 0.7 μsec pulse produced is inverted by 7/7A11 and sets the bistable 7/7A12. 7/7A13 causing $\overline{41REQ}$ to go false. $\overline{41REQ}$ causes a true <REQUEST> signal to be placed on the peripheral interface lines via the transmitter elements on boards 12, 14, 17 and 19 (Figure 8).

When the data has been accepted by the peripheral device it makes the <RESPONSE> line true. This signal is received on board 12, 14, 17 or 19 (Figure 8) and after two inversions is gated with the M signal generated by the channel selection logic (see para. 3.5). $\overline{RESPA}$ or $\overline{RESPB}$ goes false and fed to 5/1A13 causes $\overline{RESP}$ to go false and 5/2A11 to generate the 0.4 μsec PREP* pulse.

The PREP* pulse primes the control counter (see para. 3.7.3) and also causes the PREP and $\overline{PREP}$ pulses to be produced.

$\overline{PREP}$ resets the bistable 4/7B11, 4/7B12 causing TRANSFER to go false and hence OUTA goes false to remove the data gating signal.

At the end of the PREP* pulse, 5/2A13 is triggered to introduce a delay of 0.4 μsec before the 0.4 μsec COUNT pulse is generated by 5/4A11. COUNT sets the control counter, as described in para. 3.7.3 so that A goes false and B true.

When the COUNT signal goes false, a 0.4 μsec DONE pulse is generated by 5/4A13. DONE fed to 7/2A11 causes the bistable 7/7A12, 7/7A13 to be reset and $\overline{41REQ}$ to go true. The <REQUEST> signal to the peripheral goes false. DONE is also gated with $\overline{FULL}$ at 4/7B13 to set the Transfer bistable.

3.9.4 Second Transfer

TRANSFER is gated with OUTPUT at 3/1A12 causing

OUT to go true. OUT and B gated at 11/6B12 (Figure 5) cause OUTB to go true and gate DATA7 to DATA 12 from the buffer register onto the peripheral interface lines <DATA OUT1> to <DATA OUT6>.

TRANSFER is again gated with $\overline{C}$ and $\overline{RESP}$ at 7/4B11 causing 7/2B13 to generate a 0.7 μsec pulse and initiate the sending of a true <REQUEST> signal to the peripheral devices.

The peripheral accepts the second six bits of the word and then makes its <RESPONSE> line true.

A similar sequence to that described in para.3.9.3 takes place on receipt of the true <RESPONSE> signal. $\overline{RESPA}$ or $\overline{RESPB}$ goes false to cause 5/2A11 to produce the PREP*, PREP and $\overline{PREP}$ pulses. The control counter is primed and TRANSFER reset false. The COUNT pulse changes the control counter so that B goes false and C true.

The DONE pulse causes the <REQUEST> signal to go false and sets TRANSFER true.

3.9.5 Third Transfer

TRANSFER is gated with OUTPUT at 3/1A12 causing OUT to go true. OUT and C gated at 11/3B13 (Figure 5) causes OUTC to go true and gate the DATA1 to DATA6 signals from the buffer register onto the peripheral interface lines <DATA OUT1> to <DATA OUT6>.

TRANSFER is gated with $\overline{RESP}$, C and REQ at 7/3A12 causing 7/2B13 to generate a 0.7 μsec pulse to initiate the sending of a third true <REQUEST> signal to the peripheral device.

A true [PR] signal was sent to the processor, when the RS pulse was generated, as described at the end of para.3.9.2. After the receipt of this signal the processor makes [SOP] false. This causes the

RSRY pulse to be generated by 3/4A13 and the bistable 6/4B12, 6/4B13 is reset so that [PR] is false. The processor must have made the [SOP] signal true for the next transfer before the third <REQUEST> signal can be produced as REQ is one of the signals gated at 7/3A12.

After accepting the final six bits of the word, the peripheral makes its <RESPONSE> line true.

3.9.6 Start of Next Cycle

On receipt of the <RESPONSE> signal, $\overline{\text{RESPA}}$ or $\overline{\text{RESPB}}$ goes false to cause 5/2A11 to produce the PREP*, PREP and $\overline{\text{PREP}}$ pulses. The control counter is primed and TRANSFER reset to false.

PREP is gated with C and OPQ at 4/5A11 causing $\overline{\text{CLEAR/1}}$ and $\overline{\text{CLEAR/2}}$ to go false for 0.4 μsec. These pulses are fed to the buffer register to reset the bistables to a known state.

The COUNT pulse sets the control counter so that C is false and FULL true.

When the DONE pulse occurs it is gated with FULL and OUTPUT at 4/5A13 to set the Free bistable.

As described in para.3.9.5, [SOP] must be true for the next transfer before the current cycle is completed. Therefore when FREE goes true it is immediately gated with SEND and REQ to produce the CLEAR* pulse from 4/2A13 and initiate the next data transfer cycle, the sequence being as already described in para.3.9.2 to 3.9.6 inclusive.

3.9.7 Last Word

The central processor makes [LW] true before the [SOP] signal is sent for the last transfer. As described in para.3.9.5

[SOP] must go true before the final transfer of the previous cycle can take place.

[LW] goes true and is fed to board 1 where it is inverted twice and gated with REQ at 1/3B13. When [SOP] goes true, REQ goes true causing 1/4A13 to trigger and produce a 1.2 μsec delay pulse. At the end of this time 1/4B13 is triggered to produce a 0.5 μsec pulse to set the End bistable. END* is held false by $\overline{\text{TOK}}$ and FREE being false, and OUTPUT true, resulting in a false input to 1/2A12.

When the penultimate cycle has been completed, the DONE pulse is produced and FREE is set true to start the last cycle. At the end of the DONE pulse, all inputs to 1/2A12 are true, giving a false signal to set the End* bistable.

The last cycle is started when FREE goes true and gates with SEND and REQ at 4/6A13. The sequence is identical to that already described in paras. 3.9.2 to 3.9.5 with the exception of the sending of a true [PR] signal to the processor. When RS goes true it is inhibited at 6/1B13, by $\overline{\text{END}}$ being false and a $\overline{\text{SETRY}}$ signal is not produced. This means that the [SOP] signal remains true throughout the entire transfer cycle.

At the start of the third transfer C, END* and TRANSFER gated at 7/4B13 cause a true <END> signal to be sent to the peripheral.

At the end of the third transfer to the peripheral, the DONE pulse is generated. This sets FREE true and also gates with FULL and END* at 3/5A11 to reset the Send bistable. A further cycle is therefore inhibited. DONE is also gated with FULL, END* and OPQ at 6/2A12 causing $\overline{\text{SETRY}}$ to go false and send a true [PR] signal to the processor.

The processor makes [SOP] false and hence REQ goes false. This signal resets the bistable 3/7A12, 3/7A11 causing $\overline{\text{INH I/O}}$ to go true so that a SET I/O pulse can be generated by the next [SOP] or [SIP] signal. REQ going false also triggers 3/4A11 to produce a 0.4 μsec pulse which is inverted and used to trigger 3/4A13. A 0.4 μsec RSRY pulse is produced which is inverted by 6/4B11 and used to reset bistable 6/4B12, 6/4B13 causing [PR] to go false.

3.10 Repetitive Unpacked Output

3.10.1 Continuous Transfer

It can be seen from the timing diagrams in Figure 6 that the output of data to the peripheral follows the same pattern as in the packed mode, but as only eight data bits are involved, the transfer from the buffer register to the peripheral is carried out in one operation.

The initial setting of the control logic is as described for the packed repetitive mode in para.3.9.1.

[OS7] is false causing PACKED to be false and UNPACKED true, so that when the CLEAR* pulse is produced, the control counter is set as described in para.3.7.2 so that C and $\overline{\text{FULL}}$ are true.

When TRANSFER goes true, OUT goes true and is gated with C at 11/3B13 (Figure 5) causing OUTC to go true. The outputs of the buffer register bistables, DATA1 to DATA8, are gated with OUTC at 11/1A13 etc. to place the information on the $\overline{\text{DOUT1}}$ to $\overline{\text{DOUT8}}$ lines. This information is fed to the peripheral interface lines via the transmitter elements on boards 13, 15, 18 and 20 (Figure 7).

After the peripheral has accepted the data it sends a true <RESPONSE> signal to the IMU which causes the control counter to be stepped making C false and FULL true.

The DONE pulse is gated with FULL and OUTPUT at 4/5A13 causing FREE to be reset to a true level. This allows the next cycle to be started by FREE, SEND and REQ gating at 4/6A13.

3.10.2 Last Word

The central processor makes [LW] true before the [SOP] signal is sent for the last transfer. When [SOP] goes true it causes 1/4A13 to produce a 1.2 μsec pulse which initiates the resetting of bistable 1/6A13, 1/5A12 making $\overline{\text{END}}$ false.

At the end of the penultimate cycle, FREE is reset to true, so that when the DONE pulse is finished the bistable 1/2B13, 1/2B11 is reset making END* true. The final transfer is then as described for a single unpacked output in paras. 3.8.2 to 3.8.5 inclusive.

3.11 Single Unpacked Input

3.11.1 Initial Setting

In this mode of operation an 8-bit character is input to the central processor from a peripheral device. The processor makes [OS10], [OS11] and [LW] true and the appropriate signals from [OS1], [OS2] and [OS3] are made true to select the required channel (see para. 3.5). A typical waveform diagram is shown in Figure 6.

When [SIP] goes true it is inverted twice to give a true IPREQ signal from 2/4B12.

As [OS7] is false, PACKED is false, causing the output of 2/2B12 to be true and hence $\overline{\text{SW}}$ to be true. [OS10] and [OS11] being true and [OS8] and [OS9] being false cause the output of 2/2A12 to be false. This false output is inverted by 2/2A11 and gated with $\overline{\text{SW}}$ and IPREQ at 2/1B11 causing the output to go false and REQ and IPQ to go true.

With [LW] true, when REQ goes true the output of 1/3B13 goes false to trigger 1/4A13 and produce a 1.2 μsec pulse. The end of this pulse triggers 1/4B13 to generate a 0.5 μsec pulse to set the bistable 1/6A13, 1/5A12 so that $\overline{\text{END}}$ is false. The bistable 1/2B13, 1/2B11 is also set so that END* is true.

After two inversions REQ is gated with $\overline{\text{INH I/O}}$, the true output of bistable element 3/7A12, to trigger 3/3B13 and produce the 1.4 μsec SET I/O pulse. The pulse is fed to 4/4B13 causing its output to go false and hence $\overline{\text{CLEAR/1}}$ and $\overline{\text{CLEAR/2}}$ go false. These two pulses reset the buffer register bistables on boards 8, 9 and 10 (Figure 5).

After two inversions the SET I/O pulse is gated with IPQ at 3/1A13 giving a false signal to set the bistable 3/2B12, 3/2B13 so that INPUT is true. This signal is fed to boards 12, 14, 17 and 19 (Figure 8) causing a false <OUTPUT> signal to be sent to each peripheral device.

A further inversion of SET I/O at 3/4B11 triggers 3/2A13 causing $\overline{\text{RSW}}$ to go false for 0.4 μsec. The output of 3/2A13 is inverted by 3/4B12 to trigger 3/4A13 and produce the 0.4 μsec RSRY pulse. $\overline{\text{RSW}}$ is fed to board 7 (Figure 9) to ensure that the bistable 7/5B12, 7/5B13 is set so that TOK and $\overline{\text{X18}}$ are true and bistable 7/5A12, 7/5A13 is set so that $\overline{\text{X17}}$ is true. RSRY inverted by 6/4B11 ensures that the bistable 6/4B12, 6/4B13 is set so that [PR] is false.

At the end of the SET I/O pulse, 3/2A11 is triggered to generate a 0.4 μsec pulse to set the bistable 3/1B12, 3/1B13 causing $\overline{\text{SEND}}$ to go false. This signal sets the bistable 3/7A12, 3/7A11 so that $\overline{\text{INH I/O}}$ is false and inputs to the pulse generator 3/3B13 are inhibited.

3.11.2 Data from Peripheral

SEND, the output of 3/5B13 is gated with REQ and FREE

at 4/6A13 to produce a false signal to trigger 4/2A13 and generate a 0.5 μsec CLEAR* pulse. The CLEAR* pulse is fed to board 5 (Figure 4) to set the control counter, as described in para.3.7.2, so that C is true and FULL is false.

The end of the CLEAR* pulse triggers 4/1B11 to produce a 0.4 μsec delay pulse before 4/1B13 generates a 0.4 μsec RS pulse. RS and $\overline{SW}$ gated at 4/1A12 cause $\overline{START}$ to go false to set the bistable 4/5B11, 4/5B13 so that FREE goes false. $\overline{START}$ also sets the bistable 4/7B11, 4/7B12 so that TRANSFER goes true.

TRANSFER gated with C and END* at 7/4B13 causes $\overline{41END}$ to go false. A true <END> signal is therefore sent to each peripheral via the transmitter elements on boards 12, 14, 17 and 19 (Figure 8).

TRANSFER is also gated with C, REQ and $\overline{RESP}$ at 7/3A12 causing the output to go false and trigger 7/2B13. This produces a delay pulse of 0.7 μsec before 7/3B13 is triggered to generate a 0.7 μsec pulse to set the bistable 7/7A12, 7/7A13 causing $\overline{41REQ}$ to go false. A true <REQUEST> signal is sent to each peripheral via the transmitter elements on boards 12, 14, 17 and 19 (Figure 8).

The peripheral selected by the central processor places data on the lines <DATA IN1> to <DATA IN8> and then makes its <RESPONSE> line true.

3.11.3 Data to Register

The <RESPONSE> signal is inverted twice on board 12, 14, 17 or 19 (Figure 8) and gated with the M signal derived from the channel selection logic. $\overline{RESPA}$ or $\overline{RESPB}$ goes false and these signals fed to 5/1A13 cause $\overline{RESP}$ to go false and 5/2A11 to be triggered. The 0.4 μsec pulse from 5/2A11 primes the control counter (see para.3.7.2) and causes PREP to go true and $\overline{PREP}$ false.

$\overline{\text{PREP}}$ resets the bistable 4/7B11, 4/7B12 causing TRANSFER to go false. The true <END> signal is therefore removed from the peripheral lines.

PREP and INPUT are gated at 6/2B11, the resultant false signal being inverted and gated with C at 6/3B12 to cause INC to go true.

The data signals from the peripheral are fed to the receiver elements on boards 13, 15, 18 and 20 (Figure 7) and are inverted to give signals $\overline{\text{DIN1}}$ to $\overline{\text{DIN8}}$. $\overline{\text{DIN1}}$ to $\overline{\text{DIN6}}$ are inverted on board 11 (Figure 5) and gated with INC on boards 8, 9 and 10 to load the buffer register and place the data onto the processor interface lines [IG1] to [IG6]. $\overline{\text{DIN7}}$ and $\overline{\text{DIN8}}$ are inverted at 11/3B11 and 11/3B12 respectively and gated with INC and UNPACKED at 11/4B11 and 11/4B13. The two resultant signals are passed to the processor interface lines [IG7] and [IG8] via 8/6A12 and 8/6B12.

3.11.4 Data to Processor

At the end of the PREP* pulse a delay of 0.4 μsec is produced by the pulse generator 5/2A13 before the 0.4 μsec COUNT pulse is generated by 5/4A11. The COUNT pulse steps the control counter so that C goes false and FULL true.

At the end of the COUNT pulse, 5/4A13 is triggered to produce the 0.4 μsec DONE pulse.

DONE is fed via 7/2A11 to reset the bistable 7/7A13, 7/7A12 and cause the <REQUEST> signal to the peripheral device to go false.

DONE, FULL and END* gated at 3/5A11 cause the Send bistable to be reset.

DONE, INPUT and $\overline{\text{SEND}}$ gated at 4/6B12 sets the Free bistable.

DONE, FULL and INPUT gated at 6/1B11 cause $\overline{\text{SETRY}}$ to go false and set the bistable 6/4B12, 6/4B13 to place a true [PR] signal on the processor interface line. On receipt of this signal the processor gates the data from the [IG1] to [IG8] lines and then makes [SIP] false. This causes REQ, the output of 2/7B13, to go false and trigger the pulse generator 3/4A11. The 0.4 μsec pulse is inverted by 3/4B13 and used to trigger 3/4A13 to produce a 0.4 μsec RSRY pulse. This pulse is inverted by 6/4B11 and used to reset the bistable 6/4B12, 6/4B13 causing [PR] to go false.

REQ going true also resets the bistable 3/7A11, 3/7A12 causing $\overline{\text{INH I/O}}$ to go true and remove the inhibit from the pulse generator 3/3B13.

The logic is now ready to accept the next data transfer.

3.12 Repetitive Packed Input

3.12.1 Initial Setting

In this mode [OS10], [OS11], [OS7], [BT] and the required channel selection lines are made true by the central processor. A typical waveform diagram is shown in Figure 6.

When [SIP] goes true it is inverted by 2/6B12 and 2/4B12 to give a true IPREQ signal.

As [BT] is true, $\overline{\text{BLOCK}}$ is false causing the output of 2/2B12 to be true and hence $\overline{\text{SW}}$ to be true. [OS10] and [OS11] being true and [OS8] and [OS9] being false cause the output of 2/2A12 to be false. This false output is inverted by 2/2A11 and gated with $\overline{\text{SW}}$ and IPREQ at 2/1B11 causing the output to go false and hence REQ and IPQ to go true.

After two inversions REQ is gated with $\overline{\text{INH I/O}}$, the

true output of bistable element 3/7A12, to trigger 3/3B13 and produce the 1.4 μsec SET I/O pulse. The pulse is gated with BLOCK at 1/5B11 to produce a negative pulse to set the bistables 1/6A13, 1/5A12 and 1/2B13, 1/2B11 so that $\overline{\text{END}}$ goes true and END* false.

After two inversions the SET I/O pulse is gated with IPQ at 3/1A13 giving a false signal to set the bistable 3/2B12, 3/2B13 so that INPUT is true. This signal is fed to boards 12, 14 17 and 19 (Figure 8) causing a false <OUTPUT> signal to be sent to each peripheral device.

A further inversion of SET I/O at 3/4B11 triggers 3/2A13 causing $\overline{\text{RSW}}$ to go false for 0.4 μsec. The output of 3/2A13 is inverted by 3/4B12 to trigger 3/4A13 and produce the 0.4 μsec RSRY pulse. $\overline{\text{RSW}}$ is fed to board 7 (Figure 9) to ensure that the bistable 7/5B12, 7/5B13 is reset so that TOK and $\overline{\text{X18}}$ are true, and bistable 7/5A12, 7/5A13 is reset so that $\overline{\text{X17}}$ is true.

RSRY inverted by 6/4B11 ensures that bistable 6/4B12, 6/4B13 is reset so that [PR] is false. RSRY is also gated with $\overline{\text{END}}$ and INPUT at 4/6A11 causing $\overline{\text{CLEAR/1}}$ and $\overline{\text{CLEAR/2}}$ to go false. These two pulses reset the buffer register bistables on boards 8, 9, and 10 (Figure 5). The false output of 4/6A11 also triggers 4/2A13 causing CLEAR* to go true for 0.5 μsec.

At the end of the SET I/O pulse, 3/2A11 is triggered to produce a 0.4 μsec pulse to set the bistable 3/1B12, 3/1B13 causing $\overline{\text{SEND}}$ to go false. This signal sets the bistable 3/7A12, 3/7A11 so that $\overline{\text{INH I/O}}$ is false and inputs to the pulse generator 3/3B13 are inhibited.

3.12.2 First Transfer to Register

As described in para. 3.7.3, CLEAR* and PACKED being true set the control counter so that A and $\overline{\text{FULL}}$ are true.

The end of the CLEAR* pulse triggers 4/1B11 to produce a 0.4 μsec delay pulse before 4/1B13 generates a 0.4 μsec RS pulse. $\overline{SW}$ and RS gated at 4/1A12 cause $\overline{START}$ to go false to set the bistable 4/5B11, 4/5B13 so that FREE goes false. $\overline{START}$ also sets the bistable 4/7B11, 4/7B12 so that TRANSFER goes true.

TRANSFER is gated with $\overline{C}$ and $\overline{RESP}$ at 7/4B11 causing the output to go false and trigger 7/2B13. This produces a delay pulse of 0.7 μsec before 7/3B13 is triggered to generate a 0.7 μsec pulse to set the bistable 7/7A12, 7/7A13 causing $\overline{41REQ}$ to go false. A true <REQUEST> signal is sent to each peripheral via the transmitter elements on boards 12, 14, 17 and 19 (Figure 8).

The peripheral selected by the central processor places data on the lines <DATA IN1> to <DATA IN6> and then makes its <RESPONSE> line true.

The <RESPONSE> signal is received on board 12, 14, 17 or 19 (Figure 8) and after two inversions is gated with the M signal generated by the channel selection logic. $\overline{RESPA}$ or $\overline{RESPB}$ goes false and these signals fed to 5/1A13 cause $\overline{RESP}$ to go false and 5/2A11 to be triggered. The 0.4 μsec pulse from 5/2A11 primes the control counter (see para. 3.7.3) and causes PREP to go true and $\overline{PREP}$ false.

$\overline{PREP}$ resets the bistable 4/7B11, 4/7B12 causing TRANSFER to go false.

PREP and INPUT are gated at 6/2B11, the resultant false signal being inverted and gated with A at 6/2B13 to cause INA to go true.

The data signals from the peripheral are fed to the receiver elements on boards 13, 15, 17 and 20 (Figure 7) and are inverted to

give signals $\overline{\text{DIN1}}$ to $\overline{\text{DIN6}}$. These signals are inverted on board 11 (Figure 5) and then gated with INA on boards 8 9 and 10 to load the buffer register bistables. The data is now present on the computer interface lines [IG13] to [IG18].

At the end of the PREP* pulse a delay of 0.4 μsec is produced by the pulse generator 5/2A13 before the 0.4 μsec COUNT pulse is generated by 5/4A11. The COUNT pulse steps the control counter causing A to go false and B true.

At the end of the COUNT pulse, 5/4A13 is triggered to produce the 0.4 μsec DONE pulse.

3.12.3 Second Transfer to Register

DONE is fed to 7/2A11 to reset the bistable 7/7A13, 7/7A12 causing the <REQUEST> signal to the peripheral to go false.

DONE is gated with $\overline{\text{FULL}}$ at 4/7B13 to set the TRANSFER signal true.

TRANSFER is again gated with $\overline{\text{RESP}}$ and $\overline{\text{C}}$ at 7/4B11 causing 7/2B13 to trigger and initiate the sending of a true <REQUEST> signal to the peripheral.

On receipt of the true <REQUEST> signal, the selected peripheral places a second batch of information on the <DATA IN1> to <DATA IN6> lines and again makes its <RESPONSE> line true.

As in the first transfer a true <RESPONSE> signal causes $\overline{\text{RESPA}}$ or $\overline{\text{RESPB}}$ to go false to trigger 5/2A11. The resultant PREP pulse is gated with INPUT at 6/2B11, the output being inverted and gated with B at 6/3A12 causing INB to go true.

The data signals are gated with INB to load the buffer register bistables and cause the information to be present on the processor interface lines [IG7] to [IG12].

$\overline{\text{PREP}}$ resets the TRANSFER signal false and PREP* primes the control counter.

After a delay of 0.4 μsec the COUNT pulse is generated to step the counter so that B goes false and C true.

The 0.4 μsec DONE pulse is again produced.

3.12.4 Third Transfer to Register

DONE is fed to 7/2A11 to reset the <REQUEST> signal false, and is gated with $\overline{\text{FULL}}$ at 4/7B13 to set TRANSFER true.

TRANSFER is gated with C, REQ and $\overline{\text{RESP}}$ at 7/3A12 to initiate the sending of a third true <REQUEST> signal.

The final six bits are placed on the <DATA IN1> to <DATA IN6> lines and <RESPONSE> is made true.

A true <RESPONSE> signal causes $\overline{\text{RESPA}}$ or $\overline{\text{RESPB}}$ to go false and trigger 5/2A11. The PREP pulse is gated with INPUT at 6/2B11, the output being inverted and gated with C at 6/3B12 causing INC to go true.

The data signals are gated with INC to load the buffer register bistables and cause the information to be present on the processor interface lines [IG1] to [IG6].

$\overline{\text{PREP}}$ resets the TRANSFER signal false and PREP* primes the control counter.

After a delay of 0.4 μsec the COUNT pulse is generated to step the counter so that C goes false and $\overline{\text{FULL}}$ true.

The 0.4 μsec DONE pulse is again produced.

3.12.5 Data to Processor

DONE is gated with FULL and INPUT at 6/1B11 causing $\overline{\text{SETRY}}$ to go false and set the bistable 6/4B12, 6/4B13 to place a true [PR] signal on the processor interface line. On receipt of this signal the processor gates the data from the [IG1] to [IG18] lines and then makes [SIP] false. This causes REQ, the output of 2/7B13, to go false and trigger 3/4A11. The resultant 0.4 μsec pulse is inverted and used to trigger 3/4A13 to produce a 0.4 μsec RSRY pulse. This pulse is inverted at 6/4B11 and used to reset the bistable 6/4B12, 6/4B13 causing [PR] to go false.

RSRY also gates with INPUT and $\overline{\text{END}}$ at 4/6A11 to start the next input cycle.

3.12.6 Last Word

The central processor makes [LW] true before the [SIP] signal is made true for the last transfer.

[LW] is fed to board 1 where it is inverted twice and gated with REQ at 1/3B13. When [SIP] goes true, REQ goes true causing 1/4A13 to trigger and produce a 1.2 μsec delay pulse. At the end of this line 1/4B13 is triggered to produce a 0.5 μsec pulse to set the End bistable. Since OUTPUT and DONE are false at this time, the End* bistable is also set.

The data transfer proceeds as already described in paras. 3.12.2 to 3.12.5 inclusive.

At the start of the third transfer C, END* and

TRANSFER gated at 7/4B13 cause a true <END> signal to be sent to the peripheral.

At the end of the third transfer to the register, the DONE pulse is used to reset the control logic. It is gated with FULL and END* at 3/5A11 causing the bistable 3/1B12, 3/1B13 to be reset and $\overline{\text{SEND}}$ to go true. $\overline{\text{SEND}}$, INPUT and DONE gated at 7/6B12 cause FREE to be reset true.

When [SIP] goes false at the end of the last transfer, the bistable 3/7A12, 3/7A11 is reset causing $\overline{\text{INH I/O}}$ to go true. RSRY cannot start a further cycle as $\overline{\text{END}}$ is now false.

3.13 Repetitive Unpacked Input

3.13.1 Continuous Transfer

Comparison of the timing diagrams in Figure 6 shows that the input of data to the processor follows the same pattern as in the packed repetitive mode, but as only eight data bits are involved the transfer from the peripheral to the buffer register is carried out in one operation.

Interface signals [OS11], [OS10], [BT] and the channel selection signals are made true.

The initial setting of the control logic is as described for the packed repetitive mode in para.3.12.1.

As [OS7] is false PACKED is false so that when the CLEAR* pulse is produced the control counter is set, as described in para.3.7.2, so that C and $\overline{\text{FULL}}$ are true.

After receiving the <REQUEST> signal the peripheral places information on the <DATA IN1> to <DATA IN8> lines and makes

<RESPONSE> true. The PREP pulse causes INC to go true and gate DIN1 to DIN6 into the buffer register and place the data on the [IG1] to [IG6] lines. DIN7 and DIN8 are gated with INC and UNPACKED to transfer the data to the [IG7] and [IG8] lines.

The data is then accepted by the central processor and the next cycle initiated as described in para.3.12.5.

3.13.2 Last Word

[LW] goes true before the last [SIP] signal is sent by the central processor.

The $\overline{\text{END}}$, END* and control logic is reset as described for the packed repetitive mode in para.3.12.6.

3.14 Status Word (Figure 9)

3.14.1 Interrupt Signals

The signals are received on boards 12, 14, 17 and 19, the logic is shown in Figure 9. Taking board 12 as an example, the <INTERRUPT> signals are inverted by the receiver elements 12/4B13 for channel 1 and 12/4A13 for channel 2 causing $\overline{\text{INT1}}$ and $\overline{\text{INT2}}$ to go false. Either signal via 12/3A12 causes I (1.2) to go false. The I (1.2), I (3.4), I (5.6) and I (7.8) signals are commoned up and fed to 6/6A12 causing [PI2] to go true.

When a status word input is required by the processor the $\overline{\text{INT1}}$ to $\overline{\text{INT8}}$ signals are gated with SW1 on boards 7 and 16 and the data placed on the $\overline{\text{X1}}$ to $\overline{\text{X8}}$ lines. These signals are fed to the interface lines [IG1] to [IG8] via the transmitters on boards 8, 9 and 10.

3.14.2 Attention Signals

The signals are received on boards 12, 14, 17 and 19. Taking board 12 as an example, the <ATTENTION> signals are inverted by the receiver elements 12/3B11 for channel 1 and 12/3B12 for channel 2 causing $\overline{\text{ATT1}}$ and $\overline{\text{ATT2}}$ to go false. Either signal via 12/3A11 causes A (1.2) to go false. The A (1.2), A (3.4), A (5.6) and A (7.8) signals are joined together and fed to 6/6A12 causing [PI2] to go true.

When a status word input is required by the processor the $\overline{\text{ATT1}}$ to $\overline{\text{ATT8}}$ signals are gated with SW2 on boards 7 and 16 and the data placed on the $\overline{\text{X9}}$ to $\overline{\text{X16}}$ lines. These signals are fed to the interface lines [IG9] to [IG16] via the transmitters on boards 8, 9 and 10.

3.14.3 Valid Signals

The signals are received on boards 12, 14, 17 and 19 where they are inverted and gated with the M signal derived from the channel selection logic, causing $\overline{\text{INVALIDA}}$ or $\overline{\text{INVALIDB}}$ to go false. Either signal causes the output of 7/6B11 to go true and set the bistable 7/5B12, 7/5B13 causing $\overline{\text{TOK}}$ to go true and the output of 7/5B13 to go true.

If a data transfer is in progress and <REQUEST> and 41REQ are true, the bistable 7/5A12, 7/5A13 is set so that the output of 7/5A13 is true.

When a status word is input, SW/1 gates the two true bistable outputs at 7/4A12 and 7/4A13 to place the data onto the $\overline{\text{X17}}$ and $\overline{\text{X18}}$ lines repsectively. The data is fed to the [IG17] and [IG18] lines via the transmitters on board 10.

3.14.4 Complete Signals

The signals are received on boards 13, 15, 18 and 20 where they are inverted causing $\overline{\text{COMPA}}$ or $\overline{\text{COMPB}}$ to go false. Either signal causes the output of 7/6B13 to go true.

If no transfer or a data transfer is in progress then $\overline{\text{CONTROL}}$ is true and fed to 7/6A12 will cause the bistable 7/5B12, 7/5B13 to be reset so that $\overline{\text{TOK}}$ is true.

If a repetitive control transfer is in progress then CONTROL and BLOCK are true and the bistable is not reset until FULL goes true, the output of 7/7B12 will then go false.

If a single control transfer is requested the <COMPLETE> signal is prevented from setting $\overline{\text{TOK}}$ true by the false BLOCK signal applied to 7/7B12.

When $\overline{\text{TOK}}$ is set true, the output of 7/5B13 is true so that when a status word is requested SW/1 causes $\overline{\text{X18}}$ to go false.

3.14.5 Input Status Word

To input the status word the central processor makes [OS11], [OS10], [OS7] and [SIP] true.

As [BT] is false, $\overline{\text{BLOCK}}$ is true, so that all inputs to 2/2B12 are now true and $\overline{\text{SW}}$ goes false and SW true.

$\overline{\text{SW}}$ fed to 2/1B11 prevents the REQ and IPQ signals going true, but fed to 3/6A12 causes the SET I/O pulse to be produced by 3/3B13. The SET I/O pulse fed to 4/4B13 causes $\overline{\text{CLEAR/1}}$ and $\overline{\text{CLEAR/2}}$ to go false and reset the buffer register bistables.

SW fed to 6/5A13 and 16/3B12 causes SW/1 and SW/2 to go true and gate the information onto the $\overline{X1}$ to $\overline{X18}$ lines (see Figure 9). These lines pass the data to the [IG1] to [IG18] lines via the transmitters on boards 8, 9 and 10.

$\overline{SW}$ fed to 4/4B11 causes 4/2A13 to trigger and produce the CLEAR* pulse. After a delay of 0.4 μsec the RS pulse is produced by 4/1B13. $\overline{SW}$ fed to 4/1A12 prevents generation of the $\overline{START}$ pulse.

RS is inverted by 4/1A11 and 6/1A13 and gated with SW at 6/1A12 causing $\overline{SETRY}$ to go false. The bistable 6/4B12, 6/4B13 is set causing a true [PR] signal to be sent to the processor.

The processor gates the data from the interface lines and makes [SIP] false. $\overline{SW}$ goes true and via 3/6A12 triggers 3/4A11 to produce a 0.4 μsec pulse. This is inverted and used to trigger 3/4A13 and produce the 0.4 μsec RSRY pulse.

RSRY is inverted by 6/4B11 and resets the [PR] signal false.

3.15 $\overline{TOK}$ Signal

The $\overline{TOK}$ signal is normally false and is set true by a <COMPLETE> signal, or by any <VALID> signal going false i.e. Invalid. This can occur during an input or output transfer, in either case the effect is the same.

$\overline{TOK}$ is fed to 6/1A11 and gated with REQ causing $\overline{SETRY}$ to go false and set the [PR] signal true.

$\overline{TOK}$ fed to 4/6B11 resets TRANSFER false and prevents further transfers of data to the buffer register.

$\overline{\text{TOK}}$ is also gated with END* at 3/6A13 and with $\overline{\text{SEND}}$ at 4/7A13 and is fed to 1/2A11 to hold the output of 1/5B12 at a true level.

If a repetitive transfer is in progress, the processor after receiving the true [PR] signal will make the [SIP] or [SOP] signal false and then true for the next cycle. Immediately REQ goes true, $\overline{\text{SETRY}}$ goes false to send a true [PR] signal back to the processor. This cycle continues until [LW] goes true and $\overline{\text{END}}$ is reset false and END* true. $\overline{\text{TOK}}$ and END* resets $\overline{\text{SEND}}$ true and in turn $\overline{\text{TOK}}$ and $\overline{\text{SEND}}$ resets FREE true.

$\overline{\text{TOK}}$ is reset false at the start of the next transfer cycle.

If the single transfer mode is being used, when $\overline{\text{TOK}}$ goes true the control logic is reset immediately and a true [PR] signal sent to the processor.

3.16 Reset Signals

The Reset signals are derived from the [RESET] lines from the central processor. [RESET] is fed to 1/7B11 and when the signal goes true causes $\overline{\text{RESET}}$ to go false.

$\overline{\text{RESET}}$ performs the following functions:-

(a) Cause 3/2A13 to produce the $\overline{\text{RSW}}$ pulse to ensure that $\overline{\text{TOK}}$ is set false.

(b) Causes 3/4A13 to produce the RSRY pulse to ensure that [PR] is reset false.

(c) Resets bistable 3/1B12, 3/1B13 so that $\overline{\text{SEND}}$ is true.

(d) Sets bistable 4/5B11, 4/5B13 so that FREE is true.

(e) Resets bistable 4/7B11 4/7B12 so that TRANSFER is false.

(f) Resets bistable 7/7A13, 7/7A12 so that $\overline{41REQ}$ is true.

$\overline{RESET}$ also triggers 1/6B13 to produce the 16 ms $\overline{41RESET}$ pulse. This pulse is fed to all the peripheral devices via the transmitters on boards 12 14,17 and 19.